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09/842,435	04/25/2001	Brian William Hughes	10004546-1	7471

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,435	HUGHES ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-29* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 05/24/2006 have been fully considered but they are not persuasive.

At contention is the interpretation "physical re-mapping" and also the Applicant's contention that the Eaton prior art deviates from the standard use of fuses and/or programmable memory for physically re-mapping defective memory to redundant replacement memory in favor of logically re-mapping defective memory to redundant replacement memory even though the Eaton Prior Art only teaches an interpreter for receiving logical addresses and ensuring that a logical address is rerouted to access the physical address of a redundant replacement memory used to replace a defective physical memory instead of the physical address of the defective physical memory.

The Examiner would also like to point out that "logical address" is defined as a memory location accessed by an application program in a system with virtual memory such that intervening computer hardware and/or software maps the virtual address to real (physical) memory (http://en.wikipedia.org/wiki/Logical_address).

The Examiner asserts that generally Memory includes an Address Decoder that functions to map logical addresses A_i to physical addresses PA_i using a map M: $A_i \rightarrow$

PA_i. The Examiner introduces Brown; George W. et al. (US 4577294 A, hereafter referred to as Brown) strictly as a teaching reference on how defective memory cells are mapped to redundant replacement memory cells. Col. 1, lines 56-68 in Brown teach that programmable fuses are inserted between an address decoder and memory to receive physical addresses from the Address decoder and re-map the physical address by opening the fuse to disconnect defective physical memory and physically connect redundant replacement memory. That is the programmable fuses operate to map physical addresses $PA\_defective_i$ of defective physical memory to physical addresses $PA\_redundant_i$ of redundant replacement memory using a Map T: $PA\_defective_i \rightarrow PA\_redundant_i$. The Examiner asserts that there are 613 issued patents teaching redundant replacement memory and not one of the patents that the Examiner is aware of teaches issuing of logical addresses to redundant replacement memory prior to the assignment of the redundant replacement memory to replace defective memory since applications have no business accessing redundant memory prior to the assignment of redundant memory to replace defective memory, that is, redundant replacement memory is allocated memory having only physical addresses prior to its assignment to replace defective memory. Note: providing logical addresses to redundant memory prior to its assignment to replace defective memory would dramatically increase system complexity, if it were even possible since the system would have to account for data stored in redundant memory prior to its assignment to replace defective memory and would have to be able to recognize that the various logical addresses for redundant memory after its assignment to replace defective memory were no longer in use or else

they would have to be relocated. The Examiner asserts that assigning logical addresses to memory prior to its assignment to replace defective memory is just not done.

The Examiner would like to point out that Figure 3 of Eaton teaches Address Interpreter 3-9 receives logical addresses A_i from via channel 3-7 and uses the received addresses to access memory ensuring that the logical addresses A_i are rerouted to access the physical address $PA\_redundant_i$ of a redundant replacement memory used to replace defective physical memory instead of the physical addresses $PA\_defective_i$ of defective physical memory. That is the Eaton patent effectively implements a map T': $PA\_defective_i \rightarrow PA\_redundant_i$ when memory is defective and T': $PA_i \rightarrow PA_i$ when memory is not defective for replacing defective memory so that when an application program requests access to a defective memory location using a logical address A_i, the address interpreter effectively implements the map $D(T(A_i)) = PA\_redundant_i$ when memory is defective and $D(T(A_i)) = PA_i$ when memory is not defective. The Examiner asserts that the map T' in the Eaton patent must re-map the physical address location of the defective memory to the physical address location of the redundant replacement memory otherwise it would be impossible to access the redundant memory. Therefore the Eaton patent teaches physically remapping the physical addresses $PA\_defective_i$ of defective physical memory to the physical address $PA\_redundant_i$ of a redundant replacement memory so that redundant replacement memory is accessed in place of the defective memory and the defective memory is no longer accessed.

The Examiner would like to point out that nowhere in the Applicant's specification does the applicant define the term Physical re-mapping nor does the Applicant use the terms "logical address" or "physical address" yet the Applicant goes on to argue that the Applicant's disclosure is different from the Eaton patent because the Eaton Patent teaches remapping logical addresses. That is the Applicant argues that contrary to common sense (and certainly the Eaton patent makes no suggestion of this but teaches standard Prior Art redundant replacement memory that only have physical addresses prior to reassignment for use as replacement memory) that redundant replacement memory in Eaton are assigned logical addresses $LA\_redundant_i$ so that application programs have access to store information in redundant replacement memory prior to their reassignment to replace defective memory. The Applicant argues that Eaton implements a Map S: $LA\_defective_i \rightarrow LA\_redundant_i$ when a location is defective and S: $LA_i \rightarrow LA_i$ for non-defective memory locations in the logical domain. The Examiner would like to point out that the Applicant's argument is completely absurd since application programs still would have access to $LA\_defective_i$ and since any data stored at $LA\_redundant_i$ would be destroyed. The Examiner asserts that if Eaton intended such a mapping that is so contrary to what is known and taught in the Prior Art, it would require an extensive explanation and an incredible amount of research.

However, in the interest of advancing prosecution the Examiner would like to point out that in such an arrangement, Application programs would access data via the following map T"=MS: $LA\_defective_i \rightarrow PA\_redundant_i$ when memory is defective so that the

physical addresses $PA\_defective_i$ of defective physical memory is effectively remapped to $PA\_redundant_i$ of a redundant replacement memory that is, $M(S(LA\_defective_i))=M(LA\_redundant_i)= PA\_redundant_i$ when memory is defective and $M(S(LA_i))=M(LA_i)= PA_i$ when memory is non-defective. Such an algorithm implements the following map $MSM^{-1}(PA\_defective_i) = M(S(M^{-1}(PA\_defective_i)))= M(S(LA\_defective_i)) = M(S(LA\_defective_i))=M(LA\_redundant_i)= PA\_redundant_i$ when memory is defective. If such an algorithm as the Applicant argues was implemented, such an algorithm still must effectively physically remap the physical addresses $PA\_defective_i$ of defective physical memory to $PA\_redundant_i$ of a redundant replacement memory according to the physical map MSM^{-1} since col. 2, lines 55-58 in Eaton teaches that defective memory cells are replaced meaning that the physical address $PA\_defective_i$ of the defective memory cell is no longer available and is effectively replaced with the physical address $PA\_redundant_i$ of the redundant replacement memory cell (Note: in Eaton col. 5, lines 30-40 provide an algorithm to effectively ensure that defective memory is not used again).

However, address tables 3-11 in Figure 3 of Eaton containing address information are only available to interpreter 3-9 and information submitted to interpreter 3-9 is submitted on a bus separate from bus 3-7 in Figure 3 used for logical addresses. The Examiner asserts that if the addresses in 3-11 were logical addresses the System controller 3-13 would still have access the logical addresses; hence replacement of memory would be impossible unless the system controller 3-13 had access to the addresses and kept

track of the addresses separately. However, col. 12, lines 40-43 in Eaton teach self-test and self-repair memory hence the addresses in 3-11 in Figure 3 cannot be available to outside applications and the self-test and self-repair memory must be able to repair and replace memory internally without any interference from application programs. The Examiner asserts that the address tables in Figure 3 can only store physical addresses since there is no mechanism to notify application programs which logical addresses are no longer being used and no mechanism to notify application programs which logical addresses are allocated to redundant replacement memory prior to being used to replace defective memory.

The Applicant contends, "The language of the recited motivation, namely "one of ordinary skill in the art would have recognized that using the language physically re-mapping would have provided the operation of mapping defective memory cells at a physical location to non defective replacement memory cells at a non-defective physical location," is circular in nature. The Examiner merely asserts that it is obvious to make the modification because it is obvious to achieve the result".

That is incorrect. Eaton teaches an algorithm and device for redundant replacement memory for repairing memory which explicitly require that the physical addresses $PA\_defective_i$ of defective memory cells be disabled and replaced with the physical addresses $PA\_redundant_i$ of redundant replacement memory cells. Replacement means that when an application requests access to a defective memory location at physical address $PA\_defective_i$ using logical address $LA\_defective_i$, memory reroutes

the request to a redundant replacement memory at a physical address $PA\_redundant_i$, that is, regardless of the particular algorithm for accomplishing the replacement; the physical address $PA\_defective_i$ of the defective memory cell is re-mapped to the physical address $PA\_redundant_i$ of the redundant replacement memory cell. The only thing that Eaton does not teach is the term "physically re-mapping" to describe the process of re-mapping the physical address $PA\_defective_i$ of a defective memory cell to a physical address $PA\_redundant_i$ of the redundant replacement memory cell. Eaton clearly teaches the motivation for re-mapping the physical address $PA\_defective_i$ of a defective memory cell to a physical address $PA\_redundant_i$ of the redundant replacement memory cell; to repair defective memory cells.

The Applicant contends; "Applicant does not disagree with the notion that Eaton teaches re-mapping, nor does Applicant disagree that "re-mapping" necessarily involves the substitution of one physical memory location for another physical memory location". The Examiner asserts that "the substitution of one physical memory location for another physical memory location" is physically re-mapping since substitution is a map S: $LA\_defective_i \rightarrow PA\_redundant_i$ for replacing the physical address $PA\_defective_i$ of a defective memory cell to a physical address $PA\_redundant_i$ of the redundant replacement memory cell.

In addition, the Examiner would like to point out that physical is used as an adjective to modify remapping. Adjective is defined as a word that expresses an attribute of something

(http://www.google.com/search?hl=en&lr=&defl=en&q=define:adjective&sa=X&oi=glossary_definition&ct=title) or a word to specify a thing as distinct from something else (Merriam-Webster's Collegiate Dictionary). An attribute of the substitute mapping S: $LA\_defective_i \rightarrow PA\_redundant_i$ is that it substitutes physical memory; hence the mapping S is a physical remapping since it serves to distinguish the remapping from remapping of logical addresses available to application programs.

The Applicant agrees that Eaton teaches physical re-mapping, however argues that the Applicant's physical re-mapping is different.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "The Applicant agrees that Eaton teaches physical re-mapping, however argues that the Applicant's physical re-mapping is different") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Applicant contends, "Physical remapping involves physically changing the address lines extending between memory units".

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term.

Nowhere has the Applicant even defined the term "physical re-mapping". Nowhere does the Applicant even discuss "changing the address lines extending between memory units" in the applicant's specification.

In addition, the Examiner would like to point out that physical is used as an adjective to modify remapping. Adjective is defined as a word that expresses an attribute of something (http://www.google.com/search?hl=en&lr=&defl=en&q=define:adjective&sa=X&oi=glossary_definition&ct=title) or a word to specify a thing as distinct from something else (Merriam-Webster's Collegiate Dictionary). An attribute of the substitute mapping S: $LA\_defective_i \rightarrow PA\_redundant_i$ is that it substitutes physical memory; hence the mapping S is a physical remapping since it serves to distinguish the remapping from remapping of logical addresses available to application programs.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "physically changing the address lines extending between memory units") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Applicant contends, "the Examiner introduces Morley in an attempt to modify Eaton so that its memory element address lines are physically re-mapped to a different

address space. See Current Action, pg. 6. However, such a modification would change Eaton's principle operation".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "**address lines are physically re-mapped to a different address space**". [Emphasis Added]) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Nowhere does claim 1 recite, "address lines are physically re-mapped to a different address space". [Emphasis Added]

However for the purpose of advancing prosecution, the Examiner asserts that the only thing that using a programmable fuse would change is the programmable fuse would replace memory tables 3-11 in Figure 3. The Eaton patent requires that defective memory be replaced with redundant replacement memory and that the defective memory be eliminated from use. Programmable fuses are a common and effective mechanism for implementing look-up tables for replacing redundant replacement memory and eliminating the defective memory from use and are much faster than CAM since they are direct electrical connections by design and structure eliminating the complexity of look-up tables implemented in CAM.

The Applicant contends, "The referenced citations make clear that Eaton's principle operation requires remapping physical memory locations by changing defective memory

locations in an address table, which may be a look-up table or content-addressable memory. Clearly, such "logical" re-mapping is a completely different operation than replacing the physical address lines of a memory location. As such, modifying Eaton so that it replaces the physical lines of a memory location, as the Examiner's proposes, would change the principle operation of Eaton".

The Examiner disagrees and asserts that col. 1, lines 9-12 in Eaton teach that the principle of operation is self-testing and self-repairing computer memory.

The use of programmable logic is a mechanism for self-repairing computer memory. Col. 2, lines 55-58 Eaton teaches repairing memory by replacing defective memory cells with redundant replacement memory cells. One of ordinary skill in the art at the time the invention was made would have recognized that programmable fuses accomplish the same operation of replacing defective memory cells with redundant replacement memory cells and are faster and less complex since they are electrically wired.

The Applicant contends, "The referenced citations make clear that Eaton's principle operation requires remapping physical memory locations by changing defective memory locations in an address table, which may be a look-up table or content-addressable memory".

The Examiner asserts that a programmable fuse is a means for implementing a look-up table and is substantially a look-up table.

The Applicant contends, "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings".

The Examiner asserts that programmable fuses provide direct electrical connections and substantially instantaneous look-up.

The Applicant contends, "The referenced citations make clear that Eaton's principle operation requires remapping physical memory locations by changing defective memory locations in an address table, which may be a look-up table or content-addressable memory. **Clearly, such "logical" re-mapping is a completely different operation than replacing the physical address lines of a memory location**". [Emphasis Added].

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "**replacing the physical address lines of a memory location**". [Emphasis Added]) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Nowhere does claim 1 recite, "**replacing the physical address lines of a memory location**". [Emphasis Added]

However for the purpose of advancing prosecution, the Examiner asserts that address tables, content-addressable and programmable logic are all means for implementing look-up tables to redirect access of a defective memory location to a redundant replacement memory location. Each has its own advantage. Clearly, programmable fuses provide direct electrical connections and substantially instantaneous look-up by design. Col. 5, lines 20-25 in Eaton teaches the preferred embodiment whereby "substitute address table 3-11 can have several different embodiments such as (a) a look-up table (not shown) or (b) a content-addressable memory", which clearly are listed as suggestions not limitations on the design in Eaton so that the design in Eaton encompasses any other reasonable manner of implementation. Eaton makes no suggestion whether the look-up table is implemented in memory or by direct connection programmable fuses and presents no circuit diagram for look-up tables. There is nothing in the Eaton patent that teaches away from programmable memory and there is every suggestion that Eaton encompasses any and all implementations for look-up tables including direct connection programmable fuses.

The Applicant contends, "Finally, Eaton discloses that the address table may be a look up table or a content-addressable memory, where a computer determines if a memory has been replaced by comparing addresses in the address table".

The Examiner asserts that col. 5, lines 30-40 in Eaton explicitly teaches, "Alternatively, the substitute address table 3-11 can have the form of a content addressable memory. When the host computer system accesses memory, the memory address presented is

compared with the entries in the content addressable memory. If the desired address does not match an entry of the content addressable memory (CAM), then that particular memory location has not been replaced. If the address matches an entry of the content addressable memory, then that memory cell 3-5 is a defective memory cell 3-5a that has been replaced with a replacement memory cell 3-5c and the CAM produces the address of the replacement memory cell 3-5c".

The Examiner would like to point out that Eaton only teaches "the memory address presented is compared with the entries in the content addressable memory" when "the host computer system accesses memory" only in the alternative embodiment where CAM is used. Nowhere does Eaton suggest "a computer determines if a memory has been replaced by comparing addresses in the address table"; the computer is only allowed to accesses memory and the self-repair self-test memory internally determines if a memory has been replaced by comparing addresses in the case that a CAM is used. There is no requirement for a look-up embodiment to compare addresses and there is nothing prohibiting an implementation of a look-up table using programmable fuses with direct electrical connections as is normally done in the art (see Brown; US 4577294 A for Prior Art implementation of a look-up table using programmable fuses with direct electrical connections).

The Applicant contends, "The language of the recited motivation, namely "one of ordinary skill in the art would have recognized that using the language physically re-mapping would have provided the operation of mapping defective memory cells at a

physical location to non defective replacement memory cells at a non-defective physical location," is circular in nature".

Because of the nature of the case, the Examiner is not sure how the courts will interpret the term, "logically remapping". The Examiner would like to point out that only a judge in future litigation could determine how a word will be defined. In doing a rejection, an examiner uses dictionaries and treatises to determine the meaning of a word unless the Applicant explicitly defines the term. The Examiner attempted to provide arts and a rejection that would apply independently of how the courts and Appeal Board interpret the term "logically remapping". All of the elements in the Applicant's independent claims are common knowledge building blocks for testing and repairing memory and there is plenty of motivation for combining the various arts as shown above (programmable fuses with direct electrical connections provide a simplification for circuitry and are faster than CAM since they are direct connect). Contrary to what the Applicant suggests, the Eaton patent does not teach away from any implementation, but only outlines building blocks for the design in the Eaton patent.

The Applicant contends, "As such, the Examiner equates a memory row and a memory column to a "subset." However, claim 21 recites that each subset comprises at least two linear arrays of elements".

The Examiner asserts that a column is subset of elements of a kxn matrix is a kx1 array and is linear. Likewise a row is subset of elements of a kxn matrix is a 1xn array and is linear.

The Examiner would like to point out that only a judge in future litigation could determine how a word will be defined. In doing a rejection, an examiner uses dictionaries and treatises to determine the meaning of a word unless the Applicant explicitly defines the term. The Examiner would like to point out that nowhere in the Applicant's specification does the Applicant even use the term "linear array"; hence the term only gets its standard dictionary definition based on English construction of adjectives with nouns. Adjective is defined as a word that expresses an attribute of something (http://www.google.com/search?hl=en&lr=&defl=en&q=define:adjective&sa=X&oi=glossary_definition&ct=title) or a word to specify a thing as distinct from something else (Merriam-Webster's Collegiate Dictionary).

The Applicant contends; "Eaton and Green fails to teach or suggest "successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements" as recited in claim 21".
The Examiner asserts that a column is subset of elements of a kxn matrix is a kx1 array and is linear. Likewise a row is subset of elements of a kxn matrix is a 1xn array and is linear.
Green, in an analogous art, teaches a commonly-known **order** for evaluating defective memory cells by successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements (see steps l and m in claim 16 in col. 6 of Green; Note: a column is a linear array and a

row is a second linear array which are subsets of a memory array typically found in memory arrays forming a memory segment).

The Examiner disagrees with the applicant and maintains all rejections of claims 18-29. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 18-29 are not patentably distinct or non-obvious over the prior art of record in view of the references, Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton), Harns; Timothy (US 4460997 A) and Morley; Richard E. (US 4506362 A) in view of Bair; Owen S. et al. (US 6065134 A, hereafter referred to as Bair) in view of Green; George D. et al. (US 4965799 A, hereafter referred to as Green) as applied in the last office action, filed 02/24/2006. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) in view of Harns; Timothy (US 4460997 A) in further view of Morley; Richard E. (US 4506362 A).

See the Non-Final Action filed 02/24/2006 for detailed action of prior rejections.

3. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton), Harns; Timothy (US 4460997 A) and Morley; Richard E. (US 4506362 A) in view of Bair; Owen S. et al. (US 6065134 A, hereafter referred to as Bair)

See the Non-Final Action filed 02/24/2006 for detailed action of prior rejections.

4. Claims 21-25, 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) in view of Green; George D. et al. (US 4965799 A, hereafter referred to as Green).

See the Non-Final Action filed 02/24/2006 for detailed action of prior rejections.

5. Claims 26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) and Green; George D. et al. (US 4965799 A, hereafter referred to as Green) in view of Bair; Owen S. et al. (US 6065134 A, hereafter referred to as Bair)

See the Non-Final Action filed 02/24/2006 for detailed action of prior rejections.

Conclusion

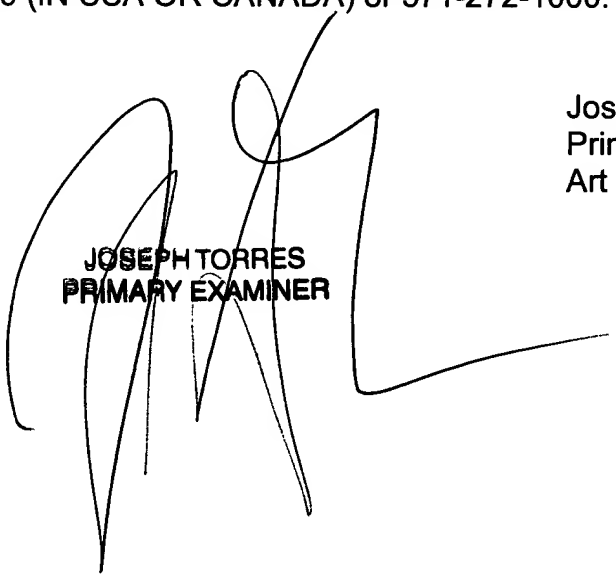
6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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